ABSTRACT OF THE DISCLOSURE

A micro-controller is connected between a hardware-based adaptive differential pulse code modulation (ADPCM) decoder and a read only memory (ROM) storing both micro-controller programming instructions and ADPCM encoded source file data. A micro-controller architecture implements time multiplexed ROM addressing driven by a two phase clock signal. In an instruction phase, a program counter supplies ROM address(es) for retrieving micro-controller programming instructions. In a decoder phase, an address counter supplies ROM address(es) for retrieving portions of the ADPCM encoded source file data. ADPCM encoded source file data extracted from the ROM in the decoder phase of the clock signal is delivered to the decoder for processing during the subsequent instruction phase of the clock signal. The selection between program counter and address counter supplied addresses for application to the ROM is made by a two phase clock signal driven multiplexer.